Bluetooth Module Datasheet

Model: AR-7111T

Version: V1.0

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Release Record

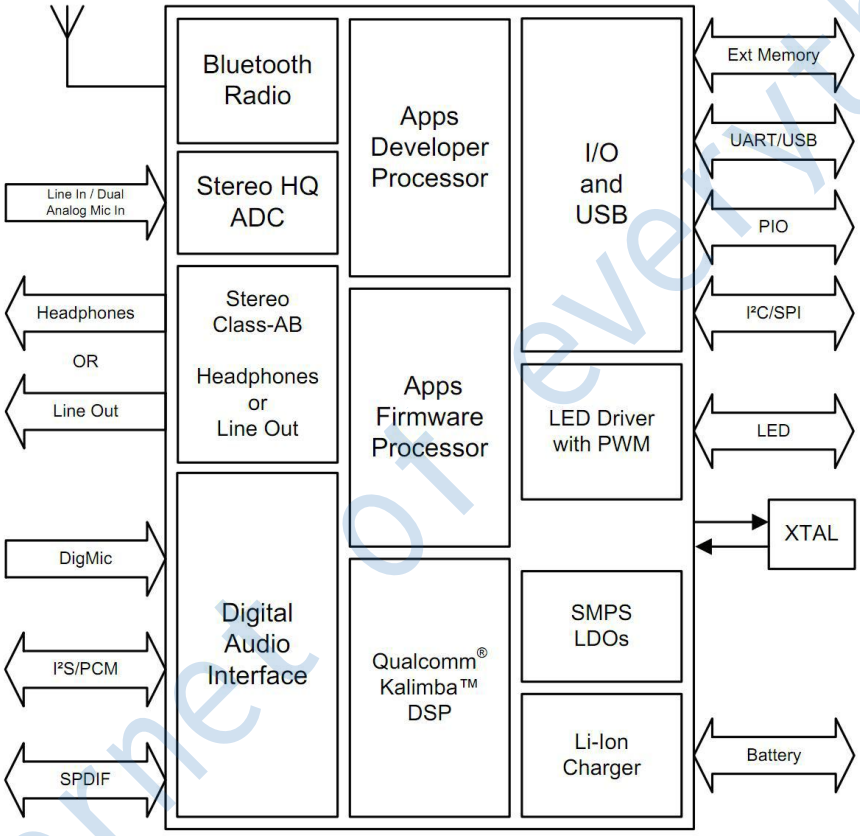
Version	Release Date	Comments
V1.0	2022-08-19	Init

List of Contents

1 Introduction

Every Interconnect Technologies introduces the pioneer of the Bluetooth 5.0 modules AR-7111T which is a high performance, cost effective, low power and compact solution. The Bluetooth module provides a complete 2.4GHz Bluetooth system based on the QCC3031 BGA chipset which is a single chip radio and baseband IC for Bluetooth 2.4GHz systems. This module is fully qualified single-chip dual mode Bluetooth@v5.0 system.

1.1 Block Diagram



1.2 Key Features

AR-7111T Features

- Qualified to Bluetooth® v5.0 specification
- 120 MHz Qualcomm® Kalimba™ audio DSP
- 32 MHz Developer Processor for applications
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms

- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- Flexible PIO controller and LED pins with PWM support
- 1-mic Qualcomm® cVc™ speaker noise reduction and echo cancellation technology
- aptX, aptX HD, aptX Low Latency, SBC, and AAC audio codecs support
- Serial interfaces: UART, Bit Serializer (I^2C/SPI), USB 2.0
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- 80-lead 8.0 x 8.0 x 0.85 mm, 0.35 mm pitch QFN

Application subsystem

- Dual core application subsystem 32 MHz operation
- 32-bit Firmware Processor:

  Reserved for system use

  Runs Bluetooth upper stack, profiles, house-keeping code
- 32-bit Developer Processor:Runs developer applications
- Both cores execute code from external flash memory using QSPI clocked at 32MHz
- On-chip caches per core allow for optimized performance and power consumption

Bluetooth subsystem

- Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy (Production parts)
- Single ended antenna connection with on-chip balun and Tx/Rx switch
- Bluetooth, Bluetooth low energy, and mixed topologies supported
- Class 1 support

1.3 Device description

- High-performance programmable Bluetooth® stereo audio SoC with Qualcomm® aptX™ audio
- Fully qualified single-chip dual-mode Bluetooth v5.0 system
- Tri-core processor architecture with low power for extended battery life

1.4 Applications

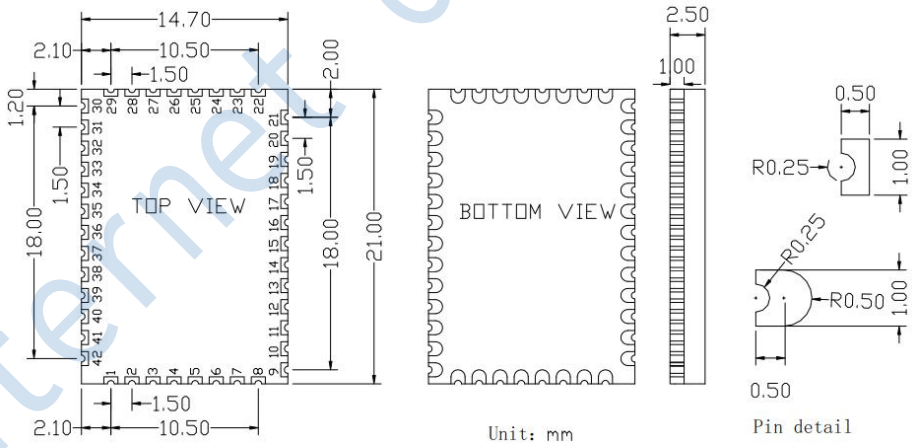
- Wired/wireless speakers

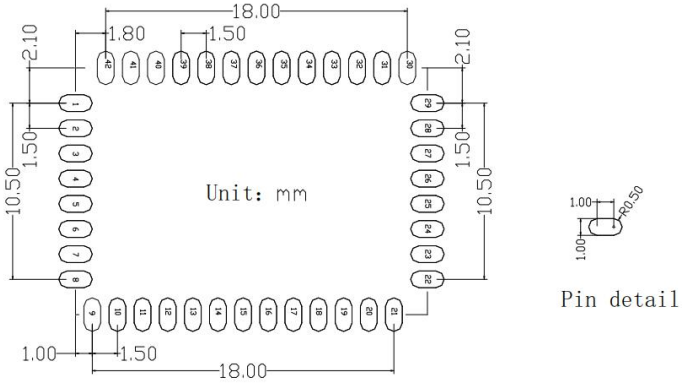
2 General specifications

Model Name	AR-7111T
Product Description	**Bluetooth 5.0 Class2 Module**
Bluetooth Standard	Bluetooth 5.0
Chipset	QCC3031 QFN
Dimension	21mm x 14.7mm
Operating Conditions	
Voltage	2.8~4.2V
Temperature	-10～+70℃
Storage Temperature	-40～+85℃
Electrical Specifications	
Frequency Range	2402～2480MHz
Maximum RF Transmit Power	9dBm
π /4 DQPSK Receive Sensitivity	-91dBm
8DPSK Receive Sensitivity	-81dBm

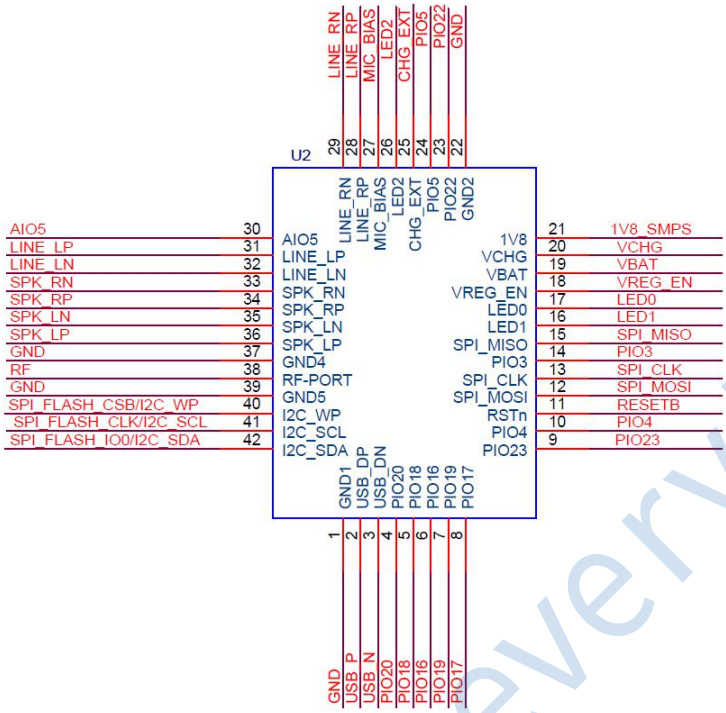
3 Pin Definition

3.1 Pin Configuration





Recommended PCB layout footprint



3.2 Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	USB_DP	Digital	USB Full Speed device D+ I/O. IEC-61000-4-2 (device level) ESD Protection.
3	USB_DN	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection.
4	PIO20	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 20. Alternative function: ■ PCM_DOUT[1]
5	PIO18	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 18. Alternative function: ■ PCM_DOUT[0]
6	PIO16	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 16. Alternative function: ■ PCM_CLK
7	PIO19	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 19. Alternative function: ■ PCM_DIN[0]
8	PIO17	Digital: Bidirectional with programmable	Programmable I/O line 17. Alternative function:

		strength internal pull-up/pull-down	■ PCM_SYNC
9	PIO23	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 23.
10	PIO4	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line4. Alternative function: ■ TBR_MOSI[1]
11	RESETB	Input with strong pull-up	Reset if low. Pull low for minimum 5ms to cause a reset.
12	SPI_MOSI	Bidirectional with strong pull-up	SPI_MOSI: Debug SPI data input Alternative function:-I2S_SD_IN:I²S synchronous data input
13	SPI_CLK	Bidirectional with strong pull-down	SPI_CLK: Debug SPI clock Alternative function:-I2S_SCK: I²S synchronous data clock
14	PIO3	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line3. Alternative function: ■ TBR_MISO[2]
15	SPI_MISO	Bidirectional with strong pull-down	SPI_MISO: Debug SPI data output Alternative function:- I2S_SD_OUT: I²S synchronous data output
16	LED1	Open-drain output	digital input or open drain LED output.
17	LED0	Open-drain output	digital input or open drain LED output.
18	VREG_EN	Analogue	Transceiver input/output line
19	VBAT	Supply	Battery voltage input.
20	VCHG	Supply	Charger input to Bypass regulator.
21	1V8_SMPS	Supply	1.8V Power supply output
22	GND	Ground	Ground
23	PIO22	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line 22.
24	PIO5	Digital: Bidirectional with programmable strength internal pull-up/pull-down	Programmable I/O line5. Alternative function: ■ TBR_MISO[1]
25	CHG_EXT	Analogue	External charger transistor current control. Connect to base of external charger transistor as per application schematic.
26	LED2	Open-drain output	digital input or open drain LED output.
27	MIC_BIAS	Analogue	Mic bias output.
28	LINE_RP	Analogue	Alternative function: ■ Differential audio line input

			right,positive
29	LINE_RN	Analogue	Alternative function: ■ Differential audio line input right,negative
30	AIO5	Analog or digital input	General-purpose analog
31	LINE_LP	Analogue	Alternative function: ■ Differential audio line input left,positive
32	LINE_LN	Analogue	Alternative function: ■ Differential audio line input left,negative
33	SPK_RN	Analogue	Alternative function: ■ Differential right line output, negative
34	SPK_RP	Analogue	Alternative function: ■ Differential right line output, positive
35	SPK_LN	Analogue	Alternative function: ■ Differential left line output, negative
36	SPK _LP	Analogue	Alternative function: ■ Differential left line output, positive
37	GND	Ground	Ground
38	RF	RF	Bluetooth transmit/receive.
39	GND	Ground	Ground
40	SPI_FLASH_CSB/I2C_WP		
41	SPI_FLASH_CLK/I2C_SCL		
42	SPI_FLASH_IO0/ I2C_SDA		

4 Interface Description

AR-7111T supports the following Host Interfaces:

- USB Device
  - ☐ Full Speed (12 Mbps)
  - ☐ Multiple IN and OUT endpoints, allocable individually
  - ☐ Charging support
- UART
  - ☐ Supports H4 and BCSP HCI interfaces or raw UART to application

- 2 x Bit Serializers that are configurable independently as ☐ I² C Master

  ☐ SPI Master

These host interfaces can operate concurrently, subject to pin multiplexing constraints, between the UART, SPI, and I²C.

Host Interface signals for UART, SPI and I²C go via a PIO mux with a further multiplexing implemented at the top level to the PIOs. The Host Interface subsystem must be selected as the controlling subsystem for the relevant PIOs.

5 Electrical Characteristics

5.1 Reset

AR-7111T module is reset from several sources.We suggest to use power-on reset,that means to leave the RSTn pin floating:

- RSTn pin pulled low for minimum 5ms
- Power-on reset, leaving the RSTn pin floating. It should be that it was 0V voltage at any pin before reset.
- USB charger attach reset
- Software configured watchdog timer

5.2 Power on and power off

AR-7111T module is power on from two sources:

- VREG_EN pin pulled high for minimum 100ms when VBAT pin is in the status of stable power.
- VREG_EN pin pulled high from low when VBAT pin is in the status of stable power.

The wrong timing sequence of VREN_EN and VBAT will lead to error of power on.

AR-7111T module is power off from two sources:

- VREG_EN pin pulled high for minimum 100ms when VBAT pin is in the status of stable power.
- VREG_EN pin pulled low from high when VBAT pin is in the status of stable power.

The wrong timing sequence of VREN_EN and VBAT will lead to error of power off.

5.3 I/O

The driver power voltage of all the PIO port is 1.8V inside of the module.

5.4 Battery Charger

AR-7111T module provides two kinds of battery charger controls.

The internal charger circuit can provide up to 200mA of charger circuit.

The module controls an external pass transistor which can provide 500mA of charger circuit.

5.5 USB

USB_P and USB_N can be used to updating software or USB audio.Both of them request that VCHG pin must be supplied 5V power.The two data signals do not need any resistance or capacitance.

5.6 Absolute Maximum Ratings

Rating	Minimum	Maximum	Unit
Storage Temperature	-40	85	℃
Supply Voltage			
VCHG	-0.4	5.75	V
LEDs	-0.4	4.4	V
VBAT SENSE	-0.4	4.4	V
VREG_EN	-0.4	4.4	V
VBAT	-0.4	4.4	V

5.7 Recommended Operating Conditions

Rating	Minimum	Typical	Maximum	Unit
Storage Temperature	-20	20	70	℃
Supply Voltage				
VCHG	4.75	5.00	5.75	V
LEDs	1.10	3.70	4.30	V
VBAT SENSE	0	3.70	5.25	V
VREG_EN	2.80	3.70	4.25	V
VBAT	2.80	3.70	4.25	V
PIO	1.50	1.80	1.90	V

5.8 Power consumption

Status	Current	Typical	Unit
Power off	VBAT	0.1	uA
A2DP slave mode with no load and playing peak noise	VBAT	12	mA
A2DP slave mode with two16ohm speakers and playing peak noise	VBAT	24	mA

Pause in A2DP slave mode connection	VBAT	0.5	mA
HFP slave mode with two16ohm speakers	VBAT	26	mA

6 Recommended reflow temperature profile

1) Follow: IPC/JEDEC J-STD-020 C

2) Condition:

Average ramp-up rate(217℃ to peak): 1～2℃/sec max.

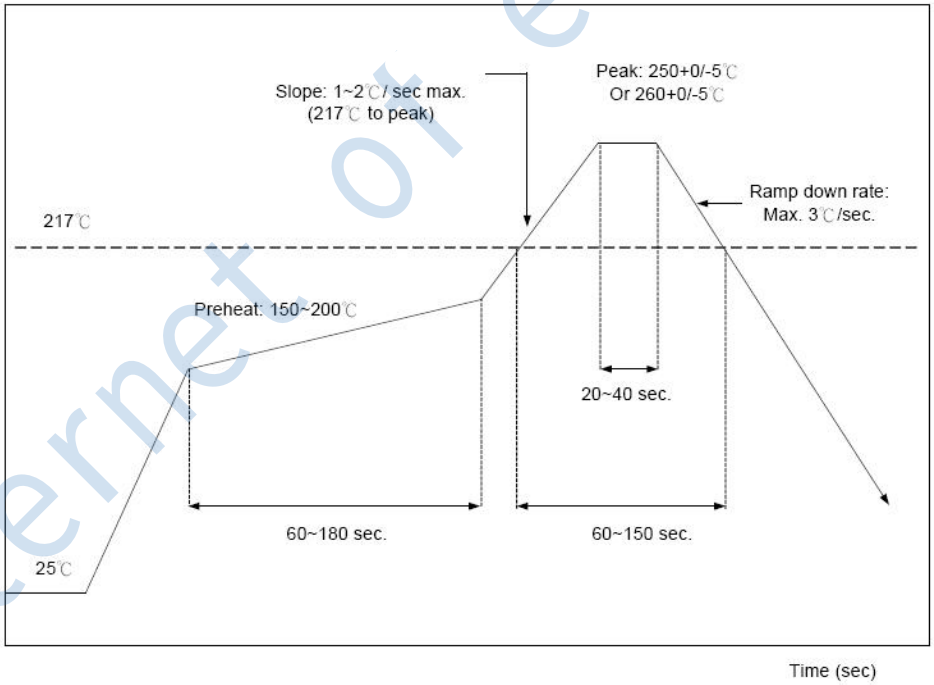
Preheat: 150～200C, 60～180 seconds

Temperature maintained above 217℃: 20～40 sec

Peak temperature: 250+0/-5℃ or 260+0/-5℃

Ramp-down rate: temperature: 8 minutes max

Cycle interval: 5 minus



CAUTION

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
3

If Blank,see adjacent
bar code label

1. Calculated sheif life in sealed bag:12 months at < 40 ℃ and < 90% relative humidity (RH)
2. Peak package body temperature: 260 ℃
   If Blank, see adjacent bar code label
3. After bag is opened.devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 168 hours of factory
   If Blank, see adjacent bar code label
   conditions ≤ 30 ℃ / 60 %
   b) stored at < 10%RH
4. Devices require bake, before mounting, if :
   a) Humidity Indicator Card is > 10 %when read at 23 ± 5 ℃
   b) 3a or 3b not met.
5. If baking is required, devices may be baked for 48 hours at 125 ± 5 ℃

Note: If device containers cannot be subjected to high temperature or shorter bake times are desired,
reference IPC /JEDEC J-STQ-033 for bake procedure

Bag Seal Date: _____ .
If Blank,see adjacent bar code label

Note:Level and body temperature defined by IPC /JEDEC J-STQ-020

The module Must go through 125℃ baking for at least 9 hours before SMT AND IR reflow process!

若拆封后未立即上线，艾瑞互联建议让下次上线前务必以 125℃烘烤 9 小时以上！

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